RECONFIGURABLE ARITHMETIC DEVICE AND ARITHMETIC SYSTEM INCLUDING THAT ARITHMETIC DEVICE AND ADDRESS GENERATION DEVICE AND INTERLEAVE DEVICE APPLICABLE TO ARITHMETIC SYSTEM

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ABSTRACT OF THE DISCLOSURE

An arithmetic device able to optimize the logic

10 level, able to prevent an increase in the component data,

able to prevent deterioration of the area efficiency as

an integrated circuit, achieving an improvement in the

operation efficiency, and achieving a reduction in the

power consumption, provided with a first selection device

15 for selecting coefficient inputs C0I to CkI in accordance

with a control signal ASEL, a second selection device for

selecting data inputs D0I to DmI in accordance with a

control signal BSEL, a third selection device for

selecting cascade inputs P0 to Pn-2 in accordance with a

20 control signal CSEL, an ALU for receiving as input the

output signals of the first to third selection devices

and performing a logic operation in accordance with

instructions of the control signals ALUMD etc., a MAC for

receiving as input the output signals of the first to

25 third selection devices and performing operation in

accordance with instructions of the control signal MACMD

etc., and a fourth selection device for selecting one of

the output signal of the ALU and the output signal of the

MAC in accordance with a control signal ESEL.

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